BUENO ELECTRIC

BEPR- 511U
Automatic Quasi-synchronizing Device
Technical Manual

V2.00

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* The specifications are subject to change without notice. When difference is found between the actual device and the specifications of the device in this manual, then the specifications shall be according to the actual device.

Contents

1 Device introduction

BEPR- 511U Digital Automatic Quasi-synchronizing Device(Hereafter to be simply called 'the device') is used for generator units incorporating into power networks ,and for substation busbars incorporating into transmission lines. The device features as fast speed, stable operating, high accuracy and high reliability. The device also has alarm functions, that is, during the connecting process, for the over-voltage, the under voltage, over frequency and under frequency on the system side, alarms can be sent out, and for the over voltage, under voltage, over frequency and under frequency on the side to be connected into the system, alarms can also be given.

1.1 Characteristic

1） Device features

- Man-machine interface friendly, operation.
- The precision of the selected measuring modules can reach to the class 0.5.
- Configured with plenty of switch quantity input, convenient external tele-siginal access
- Equipped with high precision clock chip, and equipped with GPS hardware clock synchronization circuits , is advantageous for the whole system clock synchronization
- Equipped with high speed Ethernet communication interface, and integrate the IEC 60870-5-103 standard communication protocols

1.2 Main functions

a) One device can control up to 6 generators or 6 lines for paralleling-in.

b) After settings and control words have been set up, only paralleling points are needed to be selected for each time of connecting into network.

c) Multiple closing exits form the final closing exit via "And" logic relation.

d) CB closing time angle difference is less than 0.5°.

e) Three paralleling modes are supported, that is, difference frequency paralleling, common frequency paralleling, and no-voltage paralleling.

f) Actuating can be done through digital input actuation

g) Having the function of automatic angle turning, therefore, angle turning transformer is not required. Turning angles can be selected among 30 º leading,0 º, and 30 º lagging.

h) The leading time is measured by using the CB auxiliary contact input signals.

i) For the type of device which is used for generator units, automatic frequency regulating and automatic voltage regulating can be performed, and therefore, closing time is shortened.

j) The automatic frequency and voltage regulating functions for each paralleling point can be enabled or disabled by using the control word.

k) When common frequency occurs during the generator paralleling-in process, the device can automatically give out acceleration control commands.

l) During the paralleling process, if the voltage becomes greater or less than the setting, the device will automatically block the voltage regulating function, and at the same time, closing will be blocked.

m) During the paralleling process, if the frequency becomes greater or less than the setting, the device will automatically block the frequency regulating function, and at the same time, closing will be blocked.

n) Having the functions of frequency difference (ΔF) blocking and voltage difference (ΔU) blocking closing.

0) Chinese language or English language LCD display, easy for monitoring, setting and modifying.

p) AC rated voltage: 100V or 57.74V(optional)

2 Technical data

2.1 Rated parameters

2.1.1 Rated D.C. voltage : 220V or 110V (as required)

2.1.2 Rated A. C. dat:

a) Phase voltage $100/\sqrt{3}$ V

b) Line extraction voltage 100 or $100/\sqrt{3}$ V

c) Rated frequency 50 Hz

2.1.3 Power consumption :

a) D.C circuit normal : not larger than 25W
operation: not larger than 40W

b) A.C voltage circuit not larger than 0.5VA for each phas

2.1.1 2.1.4 Status voltage :

Input voltage to CPU and signal interface	24V (18V~ 30V)
The GPS clock pulse input level	24V (18V~ 30V)
Output status (optic coupled output) permissive voltage	24V (18V ~ 30V)
driving power	150 mA

2.2 Main technical performance

2.2.1 Operating range for sampling circuits (5% tolerance)

Voltage: 0.4V～120V

2.2.2 Contact capacity

current capacity of the signal circuit contact	400VA
arc-breaking capacity of the signal circuit contact	60VA

2.2.3 Tripping and closing current

CB tripping current 0.5A~4A (as required)

CB closing current 0.5A~4A (as required)

2.2.4 Precision of elements

voltage element	less than ± 5%
Inspection synchronization angle	less than ± 1°
Timing element	less than ± 20 ms
Frequency deviation	less than ± 0.02 Hz
Slip difference value	less than ±5%

2.2.5 Precision of measuring circuits for analog variables monitoring device equipped with the special measurement sub-module :

voltage : class 0.2

2.3 Insulation property

2.3.1 Insulation resistance

Insulating resistance between active parts and passive parts or casings and electrically unrelated circuits is measured by the 500V megaohmmeter to be not less than 50MΩ for the various circuits at different levels under the normal test atmospheric conditions.

2.3.2 Strength of insulating media

Under the normal test atmospheric conditions, the protection can withstand the power frequency withstand

voltage test of 50 Hz, 2000V and 1 min without any breakdown flashover and element damages. During the test, as a voltage is applied at any tested circuit, the other circuits are inter connected and grounded with an equivalent potential.

2.3.3 Impact voltage

Under the normal test atmospheric conditions, the short-duration impact voltage test of 1.2 /50 μs standard lightning wave is done on the power input circuits. AC input circuits, output contact circuit to the ground and between circuits. The open test voltage is 5 kV.

2.3.4 Heat and moisture-proof performance

The protection can withstand the heat and moisture-proof test stipulated in GB/T 2423.9. The alternating heat and moisture-proof test is to be done at the highest temperature +40℃±2℃, the maximum humidity（93±3）%, for 48 hrs and at a cycle of 24 hrs. In 2 hrs before the test is finished, according to the requirements in section 2.3.1, the insulation resistance between the conducting circuits and external passive metals and casings and electrically unrelated parts are measured to be not less than 1.5 MΩ, the withstand voltage strength of the media not less than 75% of the voltage magnitude of the media strength test stipulated in the section 2.3.2.

2.4 Anti-electromagnetic interference

2.4.1 Electrostatic discharge

By GB/T 17626.2 1998 standard electrostatic discharge anti-interference level 4 test.

2.4.2 Radio frequency electromagnetic field radiation anti-interference

By GB/T 17626.3 1998 standard Radio frequency electromagnetic field radiation anti-interference level 3 test.

2.4.3 Electrical fast transient pulse group anti-interference

By GB/T 17626.4 1998 standard Electrical fast transient pulse group anti-interference level 4 test.

2.4.4 Surge immunity (impact)

By GB/T 17626.5 1998 standard Surge immunity (impact) anti-interference level 3 test.

2.4.5 Rf induction conduction disturbance degrees

By GB/T 17626.6 1998 standard Rf induction conduction disturbance degrees anti-interference level 3 test.

2.4.6 Power frequency magnetic field anti-interference

By GB/T 17626.8 1998 standard ower frequency magnetic field anti-interference level 5 test.

2.4.7 The pulse magnetic field anti-interference

By GB/T 17626.9 1998 standard The pulse magnetic field anti-interference level 5 test.

2.4.8 Damping oscillating magnetic field anti-interference

By GB/T 17626.10 1998 standard Damping oscillating magnetic field level 5 test.

2.4.9 Oscillation wave anti-interference

By GB/T 17626.12 1998 standard Oscillation wave anti-interference level 4 test.

2.4.10 Radiation emission limit test

By GB 9254－1998 standard Radiated emission limits A class test.

2.5 Mechanical performance

2.5.1 Vibration

The protection can withstand the impact duration test of the severity class I stipulated in the section 16.2 of GB/T 7261.

2.5.2 Impact

The protection can withstand the impact duration test of the severity class I stipulated in the section 17.4 of GB/T 7261.

2.5.3 Crash

The protection can withstand the impact duration test of the severity class I stipulated in the Chapter 18 of GB/T 7261.

2.6 Environment conditions

a) Ambient temperature :

operation : -20ºC~ +55ºC .

storage : -25ºC ~ +70ºC , no exciting variables are applied at the limit value and no irreversible changes occur. The protection will operate normally after the recovery of temperature.

b) Relative humidity : maximum monthly average humidity 90 % at the lowest temperature of 25ºC, (no condensation). At the highest temperature of +40ºC, maximum humidity must not be over 50 %.

c) Atmospheric pressure : 86 ~ 106 kPa (relative altitude above sea level is less than 2 km).

3 Hardware

High reliability is fully considered both in the overall design and module design. It is reliable in program implementation signal indication and communication. Therefore in the panel-assembling operations or the installation of the protection into the switchboard, no additional AC and DC input anti-interference modules are required.

3.1 Casing structure

The physical dimensions and holing dimensions are shown in the attached drawings.

On the operation panel, there are the LCD, signal lamps and keyboard. At the lower part of the panel there are the manual tripping and closing switches, change-over switches for discriminating local and remote operations and output pressure plates for tripping and closing. No other accessories are needed in installation. Owing to its enclosed casing, water-proof, dust-free and shock-proof design will ensure its high reliability it even in the worst environmental situations.

3.2 AC module

AC modules are composed of voltage input and current input modules. There are 3 voltage input modules and 7 current input modules. The voltage input modules are constructed of the voltage converters, whose input is 100 VAC, output about 3V. The linear range is 0.4V~120V.

3.3 CPU module

The schematic diagram of CPU module is as follows :

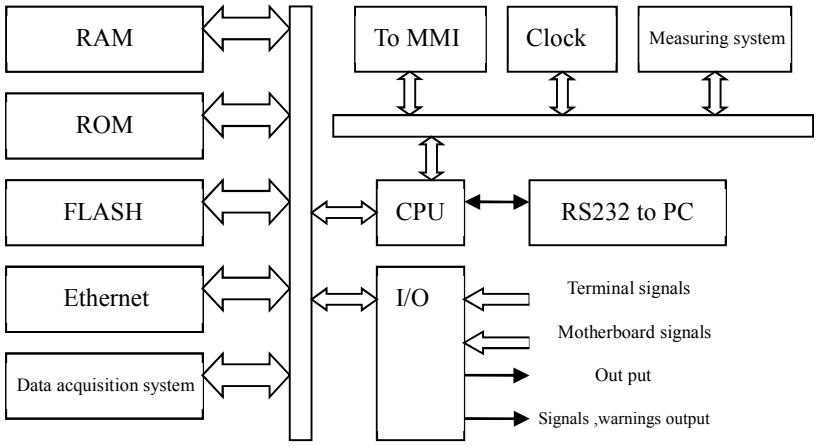


Fig 3-1 Schematic diagram of the CPU module

CPU module is composed of following elements:

1) CPU system

CPU system is composed of CPU, RAM, ROM, and Flash Memory. The high-performance 32-bit microprocessor CPU, the large capacity ROM (1M bytes), RAM (1M bytes) and Flash Memory (1M bytes) make the CPU module have a powerful data processing and recording capability and is capable of treating all

complicated faults and recording the large member of fault data. The recorded reports in Flash Memory can be 8 to 50, and events that can be recorded are 1000. And information like settings of protection can also be stored in it and will never be lost even in loss of power. Protection programs compiled by language C makes the program have a high reliability, high plant ability and high maintainability.

2) Data acquisition system

Data acquisition system is composed of two parts.

One of the data acquisition components is the 14-bit A/D converter with multi- switches and filtering circuits. The latest A/D conversion chip contains the sampling hold and synchronism circuit which features more accurate, higher in speed, and less in power consumption and more stable. No adjustable part is installed and no adjustments are necessary at site and highly reliable.

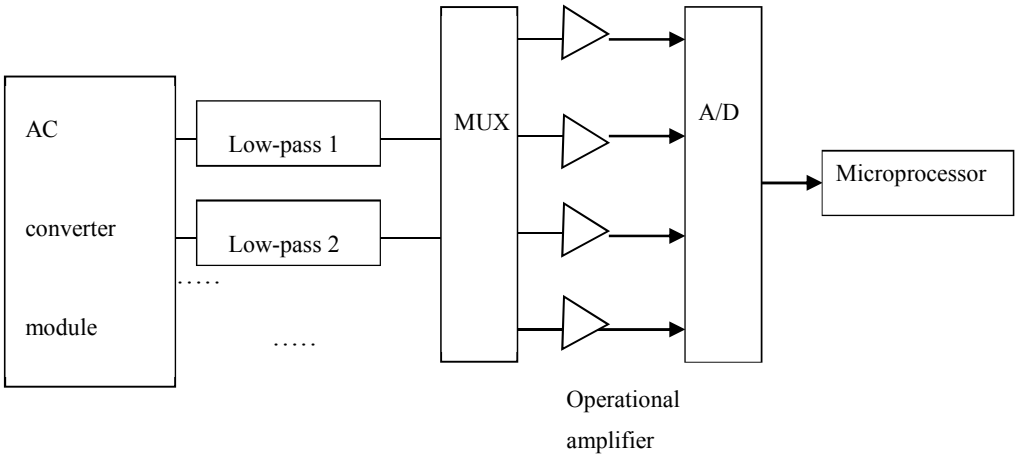


Fig 3-2 Schematic diagram of A / D system

Newly developed high precision 24-bit sample measuring chip is adopted in the measuring system, which eliminates any measuring error caused by fluctuation of frequency without any software. Once the measuring precision is set in a single time, it will automatically get the memory function and it is unnecessary to adjust it at site. This data acquisition system is provided for selection in ordering.

3) Communication

The communication module contains high speed and generally interfaced Ethernet chip which is the main communication interface for the connection of the protection with system. Generally, RJ45 acts as the communication interface UTPS wire as the media. In the special case, optic fiber communication modules are added as the interface. This nodule is provided for selection and a special order should be tendered.

4）Clock circuit

The hardware clock circuit is set up in the module

Besides, the CPU module is constructed of the multi-layer PCBs and surface-sealing technology. It is small and compact in structure. The reliability and anti-interference capability of the protection are thus greatly

enhanced. For the principle of the CPU module, refer to the appended diagrams.

See fig 3-1 for its function

3.4 Power supply module

This is a DC inverted power supply module 220V or 110V DC voltage input passing through the anti-interference filtering circuit, is converted into two groups of DC voltage: i.e. 5V, 24V, using the inversion principle. They are not in the common ground mode but in the floating ground mode without any connection with the casing.

a) +5V is used as the CPU power supply

b) 24V is used as the power supply to drive relays

c) 24V is used as the power supply for external switch-in variables.

In order to improve anti-interference ability of the power supply module, filters were added for DC inputs and 24V power supply for the outgoing terminals. For the principle of the power supply module, see the appended diagrams.

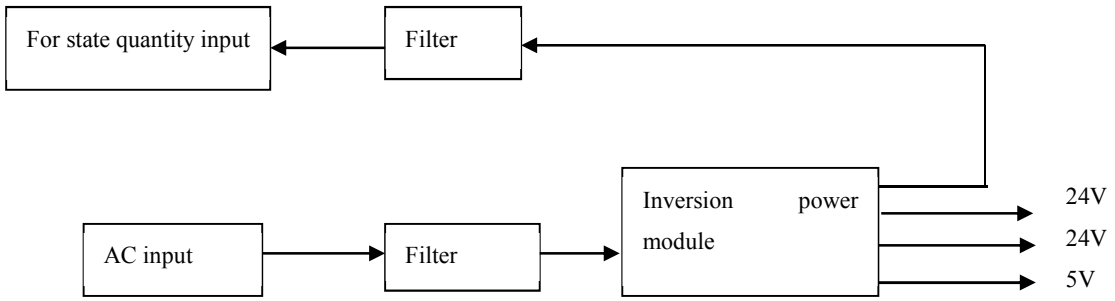


Fig 3-3 Schematic diagram of power supply module

3.5 Man-machine interaction (MMI) module

The man-machine interaction module is a single chip processor with its bus out of core. It is used to display the information from the protection's CPU and scan the key board status and then transmit it to the CPU. So the MMI module is one of its peripherals. The communication between protection's CPU and MMI is made via the SPI interface. It is high in its communication rate (up to 2Mb/s)and quite reliable. This configuration not only frees from the heavily outgoing of the CPU bus to enhance the reliability, but almost does not add the cost to lift the performance-price ratio of the protection.

The display window of the module uses the LCD unit of 4 lines and 12 Chinese characters for each line. The man-machine interface is clear to see and easy to understand. It is provided with a general keyboard operation for BEPR- series protections to make the MMI feasible and simple. At the same time, in view of the operating features of the LV protection, the sufficient lighting indication facilities are provided to make the operating information more visible. The MMI interface and feasible operating circuit have greatly riched the selection of the operating modes at site.

4 **Principle of Protection**

4.1 Synchronizing Paralleling Process

Two AC power supply systems are operating in parallel via CBs. In power systems, this kind of paralleling operation is called “Synchronizing Paralleling Operation”.

In power systems, this kind of operation is very popular and also very important, for example, the synchronizing paralleling operation between a power generator in power plants and a power network, also the synchronizing paralleling operation between a power network and another power network in substations.

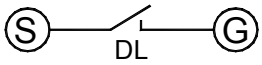


Fig. 1 Synchronizing Paralleling Operation Diagram

In the above diagram, G and S stand for two power supply systems. Supposing that they are expressed as follows respectively:

$$u_g = \sqrt{2}U_g \sin(\omega_g t + \varphi_g)$$

$$u_S = \sqrt{2}U_S \sin(\omega_S t + \varphi_S)$$

Now if we make them operate in parallel via CB DL, then the closing time moment T of DL shall in theory have the following conditions and in this way, the two power supply systems can have the minimum impulses：

$$\Delta U = | U_g - U_S | = 0$$

$$\Delta F = | F_g - F_S | = 0$$

$$\Delta\varphi = | \varphi_g - \varphi_S | = 0$$

The above three conditions are called the three main elements of synchronizing process. First capturing the time moment which can satisfy the synchronizing three main elements and then making the CBs close are the so called synchronizing process. And the point which can satisfy the synchronizing three elements is called the synchronizing point.

In the synchronizing three elements, the frequency and phase angle difference are in contradiction with each other. If the intrinsic phase angle difference of the two systems is $\Delta\varphi \neq 0$， then when equal difference element is satisfied, $\Delta\varphi$ is constant, and $\Delta\varphi$=0 is impossible forever. Only if $\Delta F = | F_g - F_S | \neq 0$， that is ,frequency difference exists, is $\Delta\varphi$=0 possible.

Actually, the synchronizing process is the process in which $\Delta\varphi$=0 is being captured, and the voltage difference and frequency difference conditions act as the restriction conditions, that is, if only ΔU and ΔF are in a certain range.

4.2 Several Synchronizing Paralleling Cases in Power Systems

4.2.1 Difference Frequency Paralleling-in

On condition that the voltages and frequencies on both sides of the paralleling point are close to each other, then the device will begin to control the CB main contact and to make it close when the phase angle difference between the two sides of the paralleling point is zero.

Operating Method: First set the control word and the settings according to the actual conditions at site, then adjust the voltage difference and frequency difference between both sides of the paralleling CB to make them satisfy the relevant conditions. In this case, if the blocking digital input is not enabled, the device will perform the difference frequency paralleling operation.

The difference frequency paralleling operation logic is as shown in the following diagram:

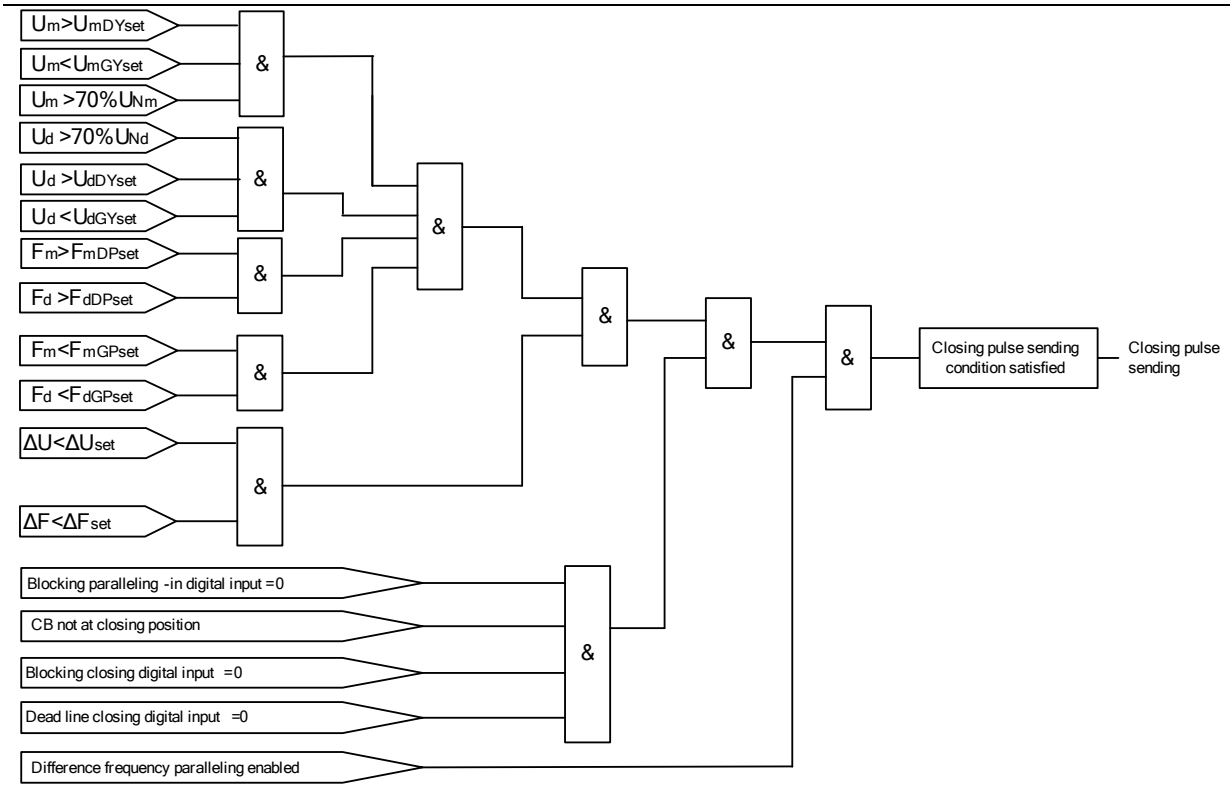


Fig 2 Difference Frequency Paralleling Operation Logic Diagram

Descriptions: Um is the actually-input system side voltage value; Ud is the actually-input voltage of the side to be paralleled in, Fm is the system side frequency, Fd is the frequency of the side to be paralleled in,ΔU is the voltage difference between the CB two sides,ΔF is the frequency difference between the CB two sides, UmDYset is the setting for the system side under voltage, UmGYset is the setting for the system side over voltag, UdDYset is the setting for under voltage of the side to be paralleled in, UdGYset is the setting for over voltage of the side to be paralleled in, FmDPset is the setting for the system side under frequency, FmGPset is the setting for the system side over frequency, FdDPset is the under frequency setting for the side to be paralleled in, FdGPset is the over frequency setting for the side to be paralleled in.Δuset is the closing permissible voltage difference setting,Δfset is the closing permissible frequency difference setting.

Calculation method for ΔU：

When the“System side voltage RMS” in the control word is selected as “57.74V”, Um100=Um×1.732

When the “System side voltage RMS”in the control word is selected as “ 100V ”,Um100=Um

When “Voltage RMS of side to be paralleled in” is selected as“57.74V”,Ud100=Ud×1.732

When “Voltage RMS of side to be paralleled in”is selected as“ 100V ”,Ud100=Ud,

$$\Delta U = | Um100 - Ud100 |$$

Um100 is the voltage value when the system side input voltage is transformed into 100V.

Ud100 is the voltage value when the input voltage of the side to be paralleled in is transformed into 100V.

4.2.2 Common Frequency Paralleling-in

On condition that the frequencies on both sides are the same and when the voltage difference and the power angle between the two sides of the CB are within the setting range, closing pulse will be sent out. At the moment when paralleling is performed, the power angle on both sides of the CB will immediately disappear, and the tidal current will reallocated. Therefore, the permissible power angle setting for the common frequency paralleling-in depends on the principle that it will not cause the relaying protection for the line to be paralleled in to operate after the system tidal current reallocation, and that it will not cause the systems on both sides of the paralleling point to lose steps.

Common frequency paralleling logic diagram is as follows:

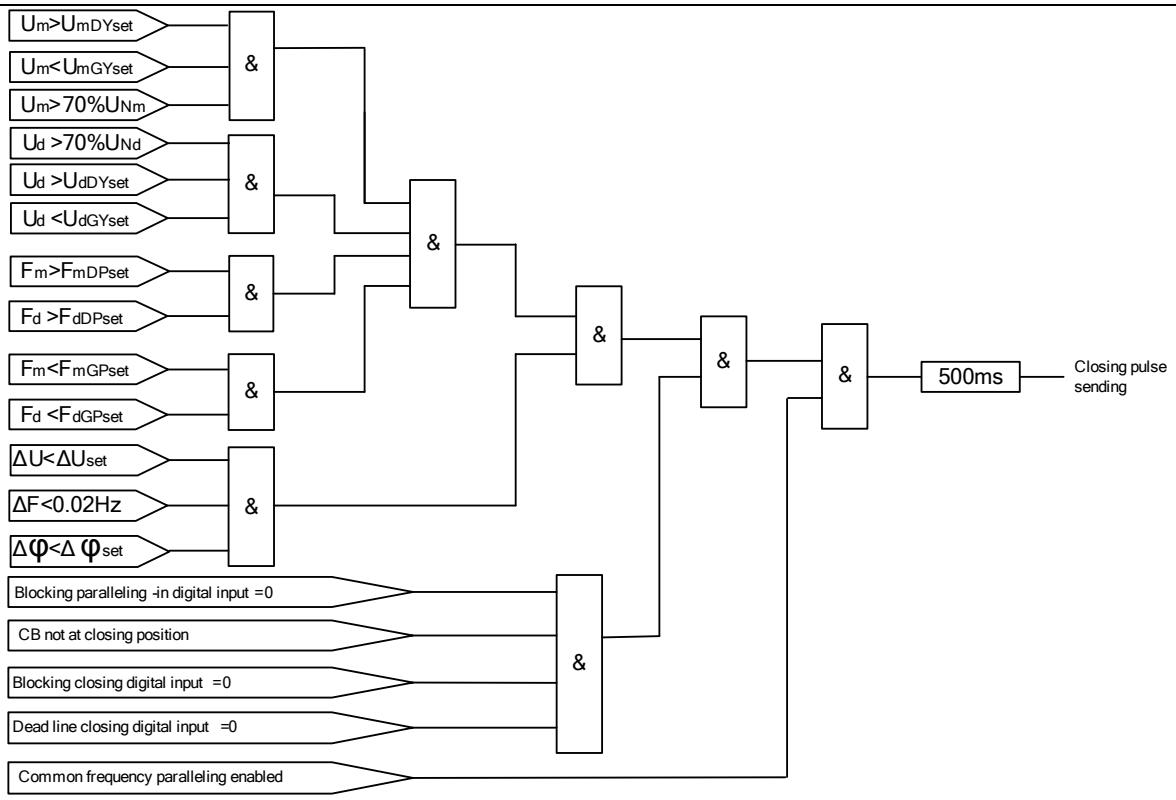


Fig. 3 Common Frequency Paralleling Logic Diagram

Descriptions: Um is the actually-input system side voltage value, Ud is the actually-input voltage value for the side to be paralleled in, Fd is the frequency of the side to be paralleled in,ΔU is the voltage difference between the two sides of the CB,ΔF is the frequency difference between the two sides of the CB, UmDYset is the under voltage setting for the system side, UmGYset is the over voltage setting for the system side, UdDYset is the under voltage setting for the side to be paralleled in, UdGYset is the over voltage setting for the side to be paralleled in, FmDPset is the under frequency setting for the system side, FmGPset is the over frequency setting for the system side, FdDPset is the under frequency setting for the side to be paralleled in, FdGPset is the over frequency setting for the side to be paralleled in,Δuset is the closing permissible voltage difference setting,Δφ is the phase angle difference between the two sides,Δφset is the common frequency paralleling permissible power angle.

Calculation method forΔU:

When “System side voltage RMS”in the control word is selected “57.74V”,

Um100=Um×1.732.

When “System side voltage RMS”in the control word is selected as “ 100V ”,Um100=Um.

When “Voltage RMS of side to be paralleled in”in the control word is selected as “57.74V”,Ud100=Ud×1.732.

When “Voltage RMS of side to be paralleled in”in the control word is selected as“ 100V ”,Ud100=Ud.

ΔU = | Um100 - Ud100 |

Um100 is the voltage value when system side input voltage is transformed into 100V

Ud100 is the voltage value when the input voltage of the side to be paralleled in is transformed into 100V.

4.2.3 Dead Line Paralleling-in

When one side or both sides of the CB to be paralleled in has(have) no voltage, the device can still perform closing operations.

No matter what type of synchronizing paralleling it is, generator type paralleling or line paralleling, it is possible to have the no voltage paralleling case. Obviously, no voltage closing is no longer the standard synchronizing process. The device only needs to judge whether the voltages on both sides of the CB DL can satisfy the no voltage condition. When the no voltage conditions are satisfied, the closing pulse will

be sent to DL.

Operation Method: Firstly set the control word and the settings according to the actual conditions at site, and then if the no voltage conditions are met and there is no blocking input, the device will perform the dead line paralleling operation.

The Dead Line Paralleling Logic is as shown in the following diagram.

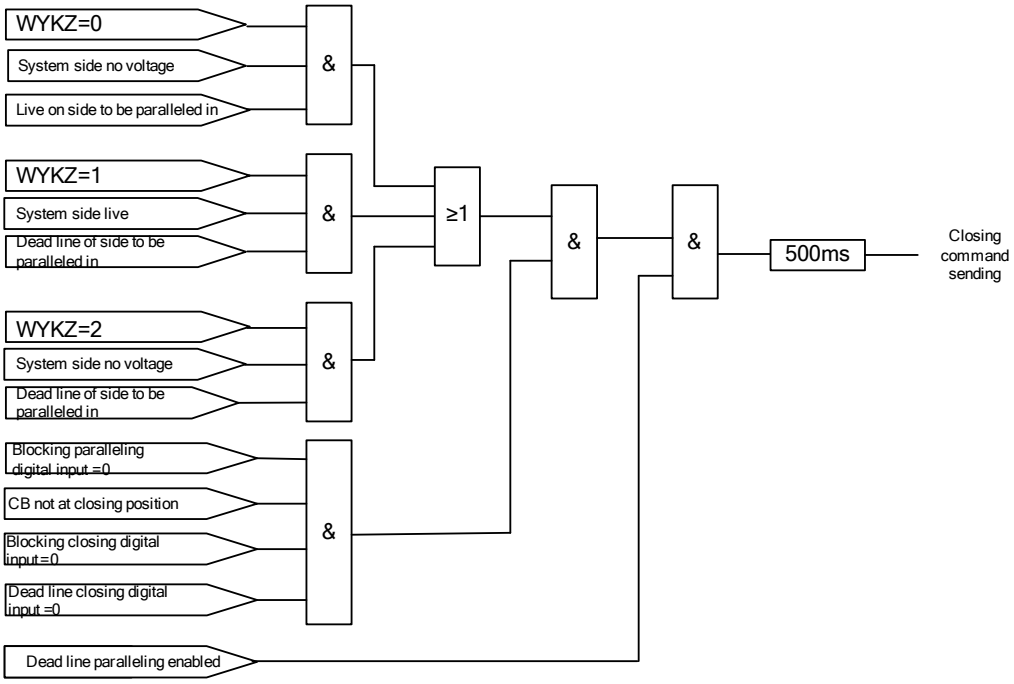


Fig. 4 Dead Line Paralleling Logic Diagram

Descriptions: WYKZ=0 means that the dead line closing is selected as the system side voltage, WYKZ=1 means that the dead line closing is selected as the voltage of the side to be paralleled in, WYKZ=2 means that the dead line closing is selected as the voltages on both sides.

When the system side input voltage is greater than 70%Un, the system live condition is satisfied; and when the input voltage is less than 10%Un，the system dead line voltage condition is satisfied.

When the input voltage of the side to be paralleled in is greater than 70%Un, the live condition of the side to be paralleled in is satisfied. When the input voltage is less than 10%Un, the dead line voltage condition is satisfied.

4.3 Operation Modes For Starting Paralleling-in

There are only one mode by which the paralleling-in can be started: This is: Digital input starting paralleling.

4.3.1 Digital Input Starting Paralleling

By the digital inputs of the device, the difference frequency paralleling, the common frequency paralleling and the dead line paralleling can be implemented.

The time sequence of the digital input starting paralleling is as shown in the following diagram（The paralleling point 2 difference frequency paralleling starting is taken as an example）

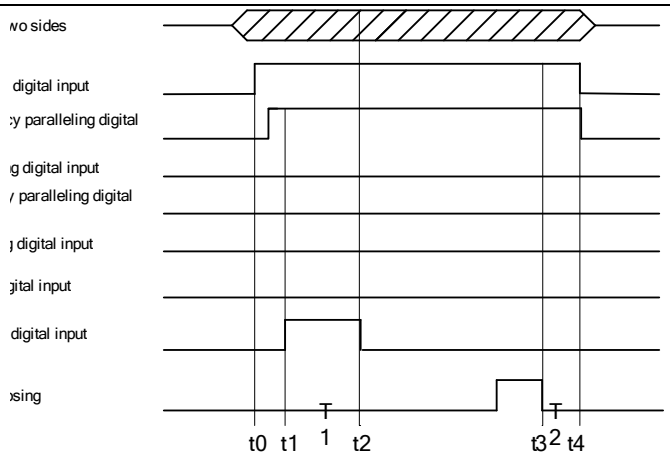


Fig.5 Time Sequence Diagram of Digital Input Starting Paralleling

The following are descriptions of how to control the device to implement the Paralleling point 2 difference frequency paralleling via the digital inputs of the device.

a) First, set the "Difference Frequency Paralleling" in the control word for Paralleling point 2 as "Enabled".

b) The control input "Paralleling point 2"（CPU module terminal 2）is valid, and the remaining 5 paralleling points are invalid.

c) The digital input operated"Difference Frequency Paralleling"（DC Module Terminal 1）is valid, the remaining digital input operated paralleling modes are invalid（Common frequency paralleling, dead line paralleling）and the dead line closing digital inputs are invalid.

d) The digital inputs for blocking paralleling and blocking closing are invalid. The CB auxiliary contact input indicates that the CB is at the tripping position.

e) After the digital input for"Starting Paralleling"changes from "Valid" to "invalid"，the device will start the paralleling process（The holding time of"Valid" is not less than 300ms）, then the"Blocking Lamp"turns off. When under voltage, over voltage, under frequency or over frequency do not appear with the system side and the side to be paralleled in, the "Alarm Lamp " turns off. When the voltage difference and the frequency difference conditions satisfy the setting requirements, the device will begin to control the CB main contact and when the phase angle difference between the two sides is zero, the main contact is closed.

f) After the device sends out the closing pulse, the digital input for controlling "Difference Frequency Paralleling"is invalid（DC Module Terminal 1），and the input for"Paralleling Point 2" is invalid（CPU Module Terminal 2）. Up to here, the paralleling process is completed.

Note： 1）The digital inputs for"Paralleling Point 2" and for "Difference Paralleling" shallbe kept valid during the paralleling process.

2）Once the device goes into the synchronizing paralleling process, any further synchronizing paralleling starting command cannot be performed whether it is via the digital inputs.

4.4 Alarm Messages

4.4.1 Alarms related to Analogue Quantities

a）System side over voltage alarm

Any time when the system side voltage becomes greater than "System side over voltagesetting", "System side over voltage alarm" will be sent out.

b）System side under voltage alarm

Any time when the system side voltage becomes less than “System side under voltage setting, “System side under voltage alarm” will be sent out.

c）Over voltage alarm for side to be paralleled in

Any time when the voltage of side to be paralleled in becomes greater than “Over voltage setting for side to be paralleled in”, “Over voltage alarm for side to be paralleled in”will be sent out.

d）Under voltage alarm for side to be paralleled in

Any time when the voltage of side to be paralleled in becomes less than “Under voltage setting of side to be paralleled in”, “Under voltage alarm for side to be paralleled in” will be sent out.

e）System side over frequency alarm

Any time when the system side frequency becomes greater than “System side over frequency setting”,“System side over frequency ”will be sent out.

f）System side under frequency alarm

Any time when the system side frequency becomes less than “System side under frequency setting”, “System side under frequency alarm”will be sent out.

g）Over frequency alarm for side to be paralleled in

Any time when the frequency of side to be paralleled in becomes greater than “Over frequency setting for side to be paralleled in”,“Over frequency alarm for side to be paralleled in” will be sent out.

h）Under frequency alarm for side to be paralleled in

Any time when the frequency of side to be paralleled in becomes less than “Under frequency setting for side to be paralleled in”,“Under frequency alarm for side to be paralleled in”will be sent out.

4.4.2 Digital input starting synchronizing alarms

The following alarms are for the case in which the digital input starts the paralleling operation. When the operation method is not correct, the device will send corresponding alarm messages and will automatically cancel the corresponding paralleling operation. The warning exit does not operate since the alarm does not have the corresponding released message. After a correct method operation is performed, the next time paralleling operation can be carried out.

a）Alarm For No Paralleling Point Starting Paralleling

When the input for “Starting Paralleling” is valid but all the “Paralleling Point”inputs are invalid, then the device will send an alarm for “No Paralleling Point Starting Paralleling”， and the paralleling operation of this time will be cancelled.

When the device detects that all the “Paralleling Points” are invalid after the paralleling operation is normally started through the digital input operation(Difference frequency paralleling, Common frequency paralleling and Dead line paralleling)and before the closing pulse is sent out, the device will automatically cancel the paralleling operation of this time.

b）Alarm For Multiple Paralleling Points Starting Paralleling

When the input for “Starting Paralleling”is valid but more than one paralleling point is valid at the same time, then the device will send an alarm for “Multiple Paralleling Points Starting Paralleling” and then the paralleling operation of this time will be cancelled.

When the device detects that more than one input for “Paralleling Points” is valid after the paralleling operation is normally started through the digital input operation(Difference frequency paralleling, Common frequency paralleling and Dead line paralleling)and before the closing pulse is sent out, the device will send out an alarm for multiple paralleling points starting paralleling, and will automatically cancel the paralleling operation of this time.

c）Alarm For Digital Input Selecting Multiple Paralleling Modes

When the input for “Starting Paralleling” is valid but more than one of the “Difference Frequency”, the “Common Frequency” and the “Dead Line Paralleling”modes are valid at the same time, then the device will send out an alarm for “Digital Input Selecting Multiple Paralleling Modes”, and will cancel the paralleling operation of this time.

When the device detects that more than one of the “Difference Frequency”, the “Common Frequency”and the “Dead Line” are valid after the paralleling operation is normally started through the digital input(Difference frequency, Common Frequency and Dead line paralleling) and before the closing pulse is sent out, the device will send out an alarm for “Digital Input Selecting Multiple Paralleling Modes” and will automatically cancel the paralleling operation of this time.

d）Alarm For Digital Input Not Selecting Paralleling Mode

When the digital input for “Starting Paralleling” is valid but none of the digital inputs for “Difference Frequency Paralleling”, “Common Frequency Paralleling” and “Dead Line Paralleling” is valid, the device will send out an alarm for “Digital Input Not Selecting Paralleling Mode”， and will cancel the paralleling operation of this time.

When the device detects that none of the digital inputs for “Difference Frequency Paralleling”, “Common Frequency Paralleling” and “Dead line Paralleling” is valid after the paralleling operation is normally started through the digital inputs and before the closing pulse is sent out（Difference Frequency Paralleling, Common Frequency Paralleling and Dead Line Paralleling）, the device will send out an alarm for “Digital Input Not Selecting Paralleling Mode”，and will cancel the paralleling operation of this time.

e）Alarm For Input of One Point Not Enabled

Select a digital input for the paralleling point and select a digital input for the paralleling mode and when the device detects that in the control word for the corresponding paralleling point, the “Digital Input Operation Paralleling” is selected as “Disabled”after the paralleling operation is started, then the device will send an alarm for “Input of This Point not Enabled” and this paralleling operation will be cancelled.。

4.4.3 All Alarms Related To Starting Paralleling Operations

The following alarm messages are for all the starting paralleling operations. When the operation method is incorrect, the device will send out alarm messages and cancel the paralleling operation of this time. The warning exit does not operate since the alarm does not have the corresponding released message. When the operation method is correct, the device will be able to perform the next time paralleling operation.

a）Alarm For Difference Frequency of One Paralleling Point Not Enabled Paralleling

When the device detects that “Difference Frequency Paralleling” in the control word for the corresponding paralleling point, has been set as “Disabled” when a paralleling operation is started through the digital input mode, the device will give out an alarm for “Difference Frequency Paralleling of this Point Not Enabled Paralleling” and will cancel the paralleling operation of this time.

b）Alarm For Common Frequency of One Paralleling Point Not Enabled Paralleling

When the device detects that “Common Frequency Paralleling” in the control word for the corresponding paralleling point, has been set as “Disabled” after one paralleling operation is started through the digital input mode, the device will give out an alarm for “Common Frequency Paralleling of This Paralleling Point Not Enabled Paralleling” and will cancel the paralleling operation of this time.

c）Alarm For Dead Line Paralleling of One Paralleling Point Not Enabled Paralleling

When the device detects that “Dead Line Paralleling” in the control word for the corresponding

paralleling point has been set as “Disabled” after one paralleling operation is started through the digital input mode, the device will give out an alarm for “Dead Line Paralleling Of This Point Not Enabled Paralleling” and will cancel the paralleling operation of this time.

d）Alarm For CB Closing Position Starting Paralleling

When the device detects that the CB is at the closing position after one paralleling operation(Difference Frequency Paralleling, Common Frequency Paralleling or Dead Line Paralleling) is started by the digital input, the device will give out an alarm for “CB Closing Position Starting Paralleling” and will cancel the paralleling operation of this time.

When the device detects that the CB is at the closing position after one paralleling operation(Difference Frequency Paralleling, Common Frequency Paralleling or Dead Line Paralleling) is started by the digital input mode, and before the device sends out a closing pulse, the device will send out an alarm for “CB Closing Position Paralleling” and will cancel the paralleling operation of this time.

4.4.4 Alarm For Operation Paralleling Point Setting Having Hidden Trouble

When paralleling point paralleling operation is started by the digital input, the device will detect the following conditions:

$2\times180\times\Delta Fset\times Tset > \delta set$

Where, Δfset is the closing permissible frequency difference setting,

Tset is the leading time setting,

Δset is the difference frequency paralleling blocing phase angle setting.

When the above condition is satisfied, the device will send out an alarm message for “Operation Paralleling Setting Having Hidden Trouble. However, at this time, the paralleling operation will not be cancelled(The descriptions here are only for reference by customers).

Analysis for Setting Hidden Trouble: In the difference frequency paralleling operation,the voltage condition satisfies the paralleling requirement, the frequency differences of both the system side and the side to be paralled in satisfy the setting requirement（but the frequency difference value is quite close toΔFset）. In this case, when the phase angle difference is equal to $2\times180\times\Delta Fset\times Tset$, the device will send out a closing pulse. However, since $2\times180\times\Delta Fset\times Tset > \delta set$, that is, the present phase angle difference is greater than the setting for “Difference Frequency Paralleling Blocking Phase Angle”, the device cannot send a closing pulse. Therefore, in this case, the setting for difference frequency paralleling blocking phase angle shall be increased or the closing permissible frequency difference setting shall be decreased.

4.5 Voltage and Frequency Regulating

The voltage and frequency regulating are only for Difference Frequency Paralleling. As for Common Frequency Paralleling and Dead Line Paralleling, voltage and frequency regulating are not carried out.

For the functions of frequency regulating and voltage regulating, customers can, according to the actual power system conditions and according to the corresponding paralleling points,select”Enabled” or Disabled”in the control words. When “Enabled” is selected, the frequency regulating and voltage regulating will be implemented. And when “Disabled” is selected, the device will not perform the frequency regulating or the voltage regulating.

The difference frequency paralleling process can be simply regarded as the process in which the voltage difference△U and the frequency difference△F are looking for the phase angle difference $\Delta\varphi=0$ within the permissible range. In order to speed up the paralleling between the system side and the side to be paralleled in, normally-speaking, according to the actual sizes of the voltage difference △U and the frequency

difference△F， the voltage U and the frequency F of the generator to be paralled in, need to be regulated so that the voltage difference△U and the frequency difference△F can very soon satisfiy the given condition requirements, in turn the difference frequency paralleling is realized. Therefore, the regulating for the voltage U and the frequency F shall also be important functions of the synchronizing device.

In the difference frequency paralleling,when the common frequency（frequency difference is less than 0.05Hz）and not same phase conditions are met, the device will send out a series of impact pulses to eliminate in time this status so that paralleling can be very soon realized.

4.6 Leading Time

The three synchronizing conditions are: Voltage Difference, Frequency Difference and Phase Angle Difference. The existing of voltage difference and frequency difference will lead to exchange of a certain amount of reactive power with a certain amount of active power which happens on both sides of the paralleling point at the moment when paralleling is done. Whether the paralleing is between a generator and a system, or between a system and another system, this kind of power exchange will have a quite big enduring ability. Therefore, in order to realize fast paralleling during paralleling process, the voltage difference setting and the frequency difference are not necessary to be confined too strictly to prevent the paralleling speed. However, for the generator paralleling case, the existing of the angle difference will lead to damnification to the generator unit, even to cause hypo-synchronizing resonance which may lead to more severe results. Therefore a good synchronizing device shall be able to complete the paralleling process when the phase angle is zero.

In difference frequency paralleling process, especially the case in which the paralleling between a generator against a system is done, the rotating speed of the generator is changing continuously with the effect of the governor. Therefore, the difference frequency of the generator against the system is not constant, but it is a derivative which includes first step, second steps or a higher step. Moreover, the paralleling point CB has an intrinsic closing time t_k， the synchronizing device must be able to send a closing command at t_k time just before the zero phase angle difference appears. In this way, paralleling with$\Delta\varphi=0°$can be realized. Or in other words, the synchronizing device shall send the closing command one angle difference φ_k before$\Delta\varphi=0°$ appears. φ_k is related to CB closing time t_k, the frequency difference F_s, the frequency difference first derivative $\frac{dF_s}{dt}$ and the frequency difference second derivative $\frac{d^2F_s}{dt^2}$. The equation is as follows:

$$\varphi_k = F_s t_k + \frac{1}{2}\frac{dF_s}{dt}t_k^2 + \frac{1}{6}\frac{d^2F_s}{dt^2}t_k^3 \cdots\cdots$$

During the paralleling process, the synchronizing needs to continuously find solutions of the equation to obtain the presently most perfect in-advance closing angle φ_k. And at the same time, the synchronizing device also continuously measures the actual phase angle difference$\Delta\varphi$ between both sides of the paralleling point CB. When$\Delta\varphi=\varphi_k$, the device will send out a closing command and in this way, accurate paralleling is realized.

4.7 Processing For Rotating Angle Transformer

Since there are a large number of Y/△ wiring transformers in the power system, and 30°phase angle difference exists between the same name phase voltages of the transformer primary side against the secondary side, therefore, when the paralleling for the generator transformer high voltage side CB is done, the secondary voltage on one side shall be turned angle by 30°if the synchronizing voltage is taken from the same name phases with the same wiring mode on the secondary side of the high voltage side and low voltage side

PTs .In the past, this function is realized by the turning-angle transformer. The second method is that the voltage is taken from phases with different wiring modes on the high voltage side and low voltage side PTs. Therefore, in order to simplify the synchronizing system wiring, BEPR- 511UMicro-processor-based Synchronizing Device is furnished with the automatic turning-angle compensation function.

Refer to the following diagram. G is a set of generator unit. The voltages on both sides of the exit CB DL are respectively from PTg which is on the side to be paralleled in and PTs which is on the Busbar side. Between DL and the generator, there is a step-up transformer B. The wiring of B is of Y/△-11（System side voltage is taken as reference and 12 Point Position is stipulated. Obviously the voltage of side to be paralleled in is at Point 11.）

The kind of Y/△-11 wiring leads to that the voltage vector diagra of the transformer high voltage side is not superimposed with the voltage vector diagram of the transformer low voltage side, but there is a difference, and the difference is 30°. If the wiring of PTg or PTs does not compensate for the 30°difference, and there is no externally equipped turning-angle transformer, then the input voltages connected into the device must have 30°difference.

This device allows this angle difference resulted from PTg and PTs not superimposing.By turning-angle compensation setting, the device will automatically turn angle to make PTg and PTs superimposed.

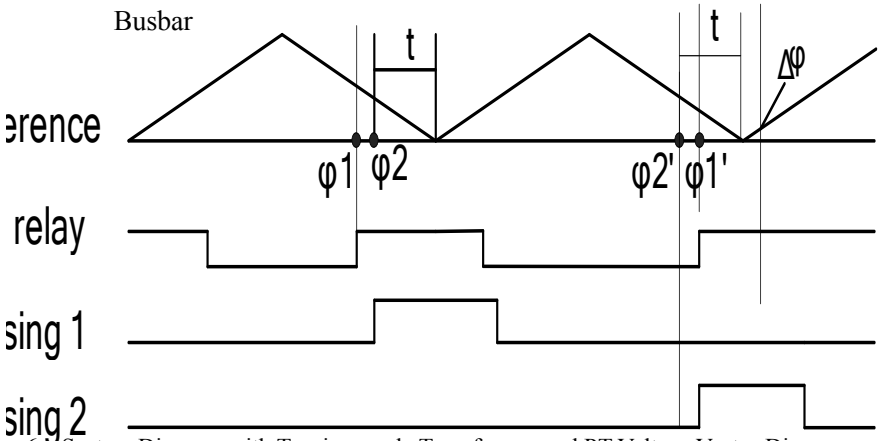


Fig. 6 System Diagram with Turning-angle Transformer and PT Voltage Vector Diagram

The turning-angle values of this device can be set for three different values: Leading 30°,0°and Lagging 30°. When turning-angle is not needed, set as 0°.

Defining of Turning Angle: Take the system side voltage as reference voltage(12 Point Position). If the voltage of the side to be paralleled in is at Point 11 position,， then Leading 30°is taken. If the voltage of the side to be paralleled in is at Point 1 position, then lagging 30°is taken.

The paralleling of the generator is by the CB DL via the Y/△-11 transformer. The synchronizing voltage is obtained by the vector relationship（when Uac is taken for the generator side）.The synchronizing voltages are given in the following table. When the transformer wiring is of Y/△-1，the synchronizing voltages are given in the following table (Uab is taken for the generator side）.

The generator is paralleled in the power network through the Y/△-11 wiring transformer.

Table 2 **Synchronizing Voltages with Y/△-11 and Y/△-1 transformer high voltage side paralleling**

Transformer wiring	PTg（Side to be paralleled in）	PTs（System side）	Phase shifting angle (Turning angle of system side)	Descriptions

Y/△-11		PTs phase voltage	0°	One side line voltage, anther side phase voltage
		PTs line voltage	Leading 30°	Line voltages for both sides
Y/△-1		PTs phase voltage	0°	One side line voltage, another side phase voltage
		PTs line voltage	Lagging 30°	Line voltages for both sides

Note: When every setting is done, a corresponding test must be performed to further confirm the correctness of the settings.

4.8 Several Points to Note For Synchronizing

4.8.1 etting Relationship betweenΔfset ,Tset and "Difference Frequency Paralleling Blocking Phase Angle"

2×180×ΔFset×Tset < setting of"Difference Frequency Paralleling Blocking Phase Angle"

Where, Δfset is the closing permissible frequency difference setting（Hz）

Tset is the leading time setting（s）

For example:ΔFset = 0.3Hz, Tset = 200ms, then 2×180×0.3×0.2=21.6º. Therefore, the setting for "Difference Frequency Paralleling Blocking Phase Angle" cannot be less than 21.6º.

4.8.2 Several Points To Note when a synchronizing blocking relay is used with the closing circuit

When a synchronizing blocking relay is connected in series with the closing circuit,the setting for "Difference Fequency Paralleling Blocking Phase Angle"must not be greater than the angle setting for the synchronizing blocking relay. The reasons for this are that（refer to the following diagram）when the blocking angle φ1 of the blocking relay is greater than the leading angle φ2 which is obtained by calculating the leading time t ,the closing command can be sent out when the phase angle difference between the two sides of the CB is equal to φ2. The CB is closed via the leading time t when the phase angle difference between the two sides of the CB is zero. When the blocking angleφ1' of the blocking relay is less than the leading angle φ2' which is obtained by calculating the leading time t, the closing command cannot be sent out when the phase angle difference between the two sides of the CB is equal toφ2'. Only when the blocking relay releases blocking, that is, when the phase angle difference between the two sides is equal to φ1'， the closing command can be really sent out. In this way, after the CB leading time t, and at the time when the CB is closed, the phase angle difference between the two sides is not zero, but equal to Δφ.

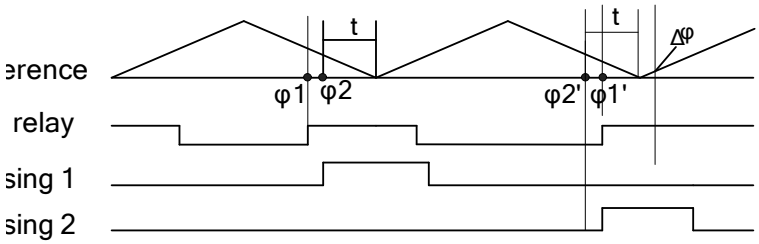


Fig 7 Synchronizing Blocking Relay in closing circuit

5 Rated Values and Setting Descriptions

5.1 List of the rated values for the BEPR- 511U Automatic Synchronizing Device and setting descriptions

Ser. No	Names of rated values	Range	Unit	Remarks
1	Control character 1	0000～FFFF	None	See the descriptions for control character
2	Control character 2	0000～FFFF	None	See the descriptions for control character
3	synchronize reset time	0.0～300.0	s	
4	Closing pulse lead time	20～999.9	ms	
5	the width of closing output pulse	0.00～99.99	s	
6	Same frequency FM pulse width	5.0～9999	ms	
7	The inherent difference of phase Angle	0.00～99.99	°	
8	Common frequency paralleling permissible power angle	0.00～99.99	°	
9	Closing permissible voltage difference	0.0～999.9	V	
10	Closing permissible frequency difference	0.00～99.99	Hz	
11	Frequency interval cycle	50～9999	ms	
12	Frequency plus witdth	50～990	ms	
13	Voltage interval cycle	50～9999	ms	
14	Voltage plus witdth	50～990	ms	
15	Rated voltage of side to be paralleled in	0.0～999.9	V	
16	Lowed voltage of side to be paralleled in	0.0～999.9	V	
17	System side rated voltage	0.0～999.9	V	
18	System side lowed voltage	0.0～999.9	V	
19	Alarm for over freuqency of side to be paralleled in	0.00～99.99	Hz	
20	Alarm for under freuqency of side to be paralleled in	0.00～99.99	Hz	
21	System side over freuqency alarm	0.00～99.99	Hz	Primary current / (Secondary current*1000)
22	System side under freuqency alarm	0.00～99.99	Hz	Primary voltage / (Secondary voltage*1000)
23	Quasi-synchronizing acceleration blocking	0.00～10.00	Hz /s	
24	Lead Angle blocking setting value	0.00～90.00	°	

Definition of control character 1 :

Bit	Meanings for 0	Meanings for 1
15	Common frequency FM: accelerated	Common frequency FM: decelerated

9、0A	System no-voltage	No-voltage in paralling side	No-voltage in all side	standby
8	Automatic frequency adjustment quit		Automatic frequency adjustment input	
7	Automatic voltage adjustment quit		Automatic voltage adjustment input	
5、6	System advance Angle 30°	System advance Angle 0°	System lagged Angle 30°	spare
4	Ring and closing is prohibited		Ring and closing is allowed	
3	Unilateral pressureless closing is prohibited		Unilateral pressureless closing is allowed	
2	In side of paralling Ue=57.7V		In side of paralling Ue=100V	
1	System voltage Ue=57.7V		System voltage Ue=100V	
0	standby		standby	

5.2 List of soft pressure plates in the BEPR- 511U Digital Automatic Quasi-synchronizing Device

Names of pressure plates	Related functions
Synchronizing	In-service and out of service of synchronizing function

6 Figures

Fig.1：BEPR- 511U Automatic Synchronizing Device back terminal diagram：

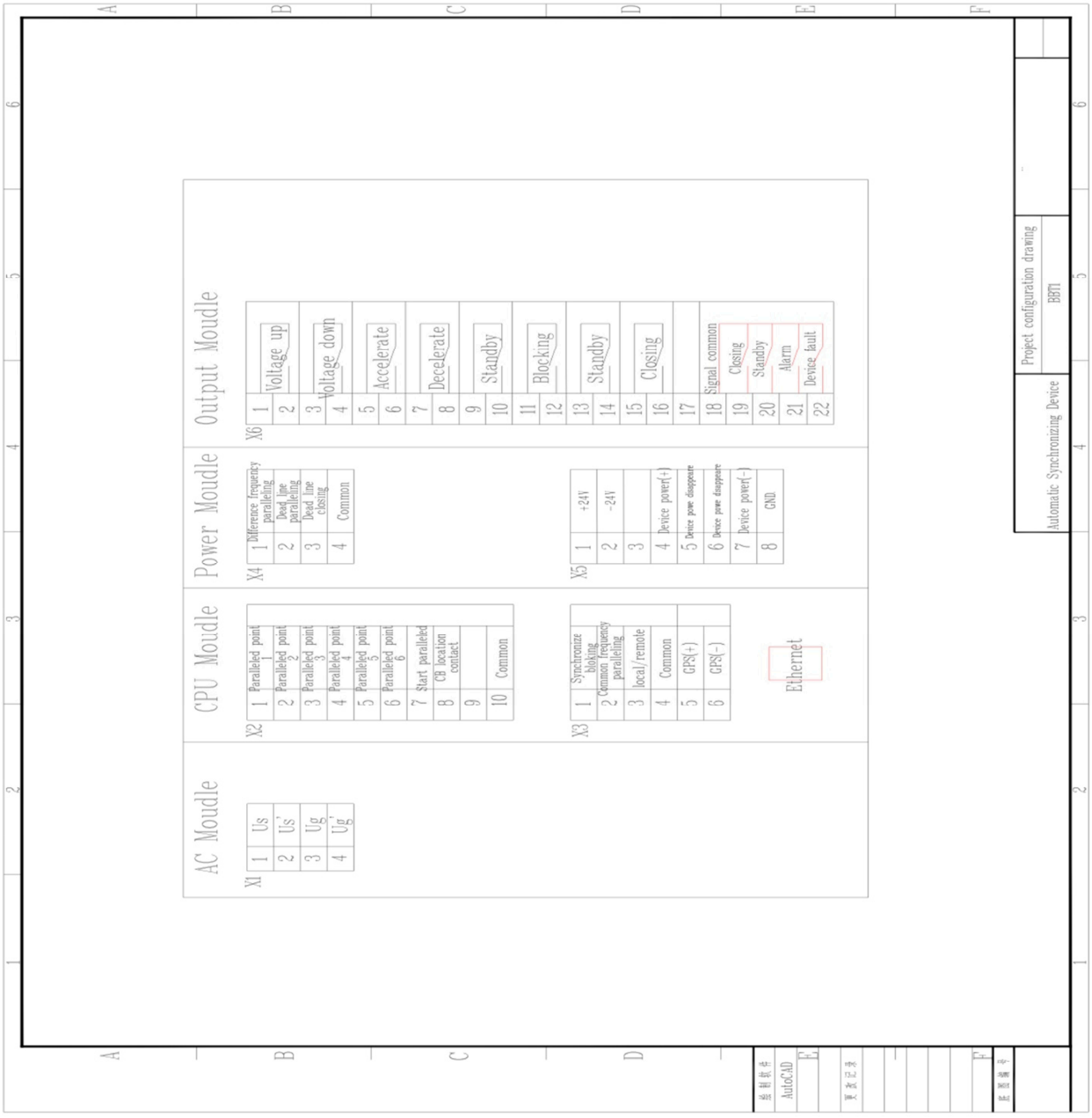
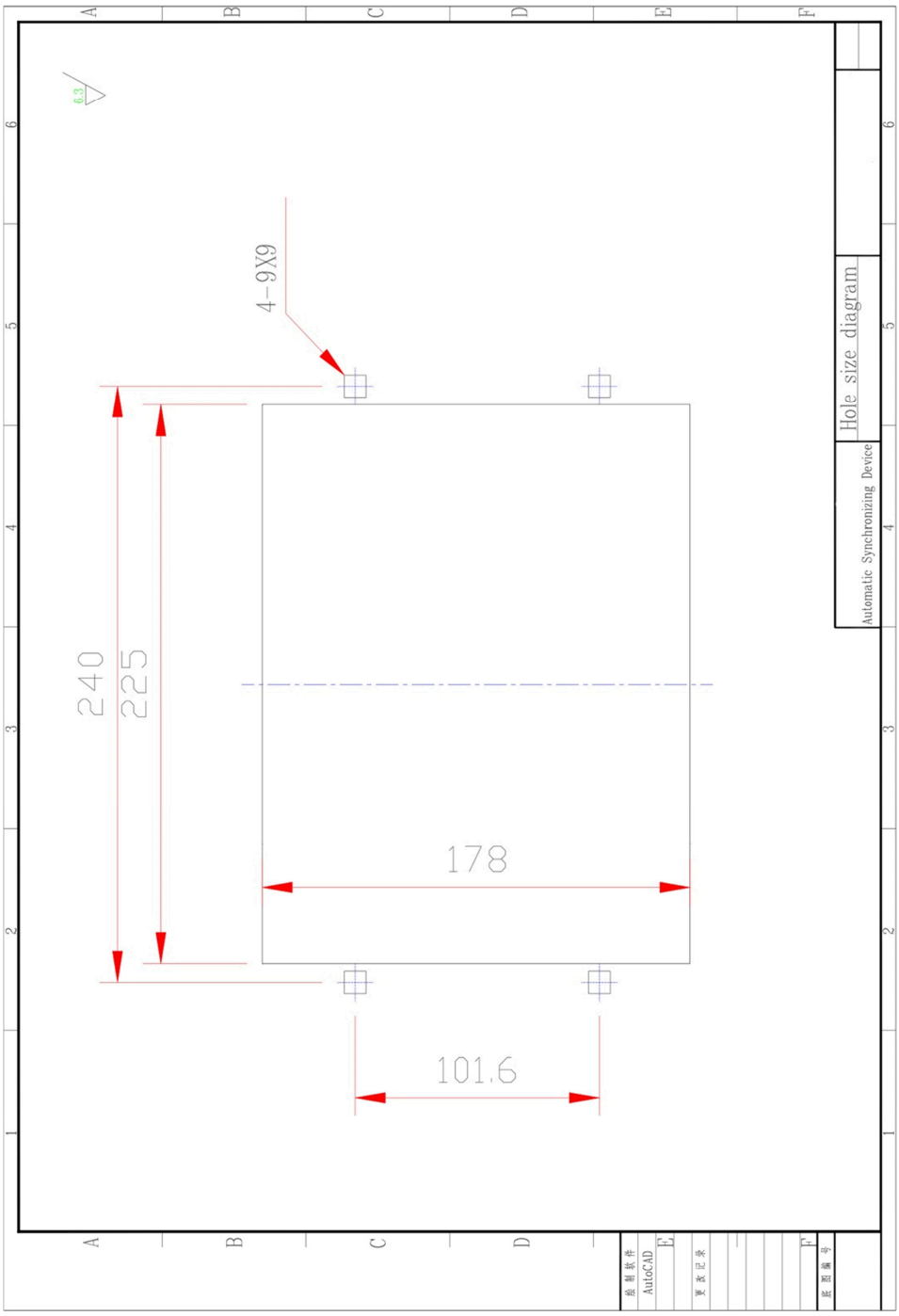


Fig.2 ： BEPR- 511U Automatic Synchronizing Device hole size diagram .


4-9X9
240
225
178
101.6
Hole size diagram
Automatic Synchronizing Device